

# Scope

This document describes the manufacturing test strategy for the Model 2412 and 2408 IPG products during various stages of the production process. The manufacturing test strategy is derived from the Model 2412 and 2408 IPG MVP (master validation plan). It will identify high level test and test system requirements for board and device level stages.

The pilot manufacturing test strategy for these products is key to processing samples for design verification test (DVT) activities, so some description of DVT will also be captured in this Plan.

# Abbreviations

DUT Device Under Test

DVT Design Verification Testing

IPG Implantable Pulse Generator

EPG External Trial Stimulator

PCB Printed Circuit Board

# References

All documents refer to the QiG Cleveland quality system and location unless otherwise noted.

IPG MVP Master Validation Plan

QAQP 0039 Inspection and Testing

QAQP 0026 Inspection, Measuring and Test Equipment Control Procedure

QAQP 0013 Software Testing and Validation Procedure

SWQP 0006 Code Management Procedure

SWWI 0004 Use of Code Management System

MEFM 0021 IPG Mechanical DFMEA

EEFM 0022 IPG Electrical DFMEA

1004467 SCS Algostim IPG PFMEA (GBM Plymouth Quality System)

QARE 0139 SCS for Pain Therapy Risk Assessment

EESP 0071 24 Channel IPG Functional Specification

SWSP0112 IPG/EPG Software Requirements Specification

SWEX0085 SCS MICS Command Design Document

SWEX0091 SCS Error Codes and Command Responses

WIXXXX Individual test outline work instruction documents

# Test Levels

The following sections describe the test levels covered by this plan.

## Test Flow

Test levels as shown in figure 1.



Figure 1: Test Flow

### PCB Test

The purpose of this test is to verify the IPG PCB is assembled to specification from the raw board and components, received in an acceptable condition, run test code when loaded and executed, and run embedded product code when loaded and configured to execute a set of board level tests.

An electrical test system with custom fixturing and software will be developed to confirm the device under test is a known good sub-assembly at this stage in the building/manufacturing of a complete IPG device. Long term a version of this test and associated test system may be deployed at the assembly vendor prior to shipment as a cycle time improvement.

This test will require the specification and building of a bed of nails fixture base and PCB inserts to interface the PCB with a custom electrical test station.

### Final Functional IPG Test

This is the final test for the fully functional IPG device prior to packaging and subsequent sterilization processes. It will verify hardware and firmware features, header attach, battery attach, feed-through attach and charging coil attach processes and components. Communication with the IPG will be made through the functioning MICS system using telemetry protocols similar to ones used in typical end user scenarios.

This test will require custom test code, a custom cartridge and custom test pins to interface the IPG device under test confirming electrical connection of all stimulation source outputs and functional operation of the magnet sensor and specifications not tested at the board level.

### Final Battery Charge/Check Test

This test will be able to verify that the IPG battery is charged within a range of battery voltage levels per specification prior to packaging and processing to sterilization and/or distribution to end users. This test method will also be able to charge or discharge a device to the specified level if it is outside of the specified range.

This test will require a custom bench-top system capable of charging/discharging multiple devices simultaneously through final packaging.

# General Test Requirements

## The following requirements apply to all test levels.

### PCB and Final Functional Tests will be performed at 37.5 +/- 0.5°C.

### Each test system will have a secure Labview/Test Stand based command environment and local storage of electronic data.

### Electronic data will be backed up on the local system and have the option of storing it on removable media as additional backup.

### Each test level will have custom fixturing but may utilize similar or same test systems as other test levels to minimize design and maintenance.

### Test report data will be tracked by device or PCB serial number.

### Test level requirements will specify tests where testing can be terminated without completing all tests.

### Each device under test will be fully tested prior to the next higher level assembly step.

### Test level requirements will specify the order of all tests.

### A backup power source will be installed on each test system to ensure that, upon power failure, a soft shutdown will allow the system to complete its test sequence for a device under test.

### Electronic records may be stored on the local test stations or a controlled access network. These records are used for backup only and are not part of a device history record (DHR).

### A sub-network may be put in place to allow test systems to be connected together in conjunction with a SQL server to store test data.

### It is not a must that the test systems interface with Oracle, but efforts will be undertaken to investigate this need.

### Long term, expected volume is 20k per year with a 90% yield at each test level. To meet this volume multiple test systems and/or shifts may be needed.

### All software will be revision controlled

## Test system components and assemblies will be controlled in various documents; bills of material, assembly drawings, specifications, electronic files, and pictures.

## Work Instructions (WIXXXX) are the next level test documents where individual test outlines, modules, and methods are identified.

## Calibration and maintenance requirements will be specified in the individual test system reference and control documents.

## If PCB testing is performed at an external vendor, same or similar methods will be generated as defined in this document.

# Test Requirement Generation

Test requirements will be based on IPG functional device specifications, the SCS System Risk Assessment, Design FMEAs, and Process FMEAs. Other requirements may be added as needed based on the judgments of the design, test and design assurance engineers.

A review of the following FMEAs will be held; Design Mechanical FMEA (MEFM 0021), Design Electrical FMEA (EEFM 0022), and Process FMEA (1004467). All mitigations identified will be implemented and verified.

A review of the SCS for Pain Therapy Risk Assessment (QARE 0139) will be held. All hazards with a severity index of 3 or above will be reviewed for electrical test mitigations not covered by the FMEAs.

A review of Functional and Design Specifications (EESP0071, SWSP0112, SWEX0085, SWEX0091) will be held. All electrical safety functions not covered by the FMEAs and Risk Assesment will reviewed for electrical test coverage and test requirements added as needed. All safety functions will be tested electrically. All other electrical functional specifications will be reviewed for electrical test coverage requirements of the design, test and design assurance engineers.

Calibrations, and programming of memory components will be performed as required to meet the functional specification.

All limits will be specified with a required resolution.

# Verification and Validation

IQ, OQ, PQ protocols will be developed and executed for each of the test systems that will perform any or all of the tests outlined in section 4, prior to product launch. Gauge R&R ANOVA methods will be referenced in determining needed accuracy and repeatability of parametric measurement systems, and captured in the IQ, OQ, and PQ protocols. A traceability matrix showing that all test requirements are verified will be included in the associated reports.

Each test module which requires an automated measurement will have acceptance or pass/fail criteria. Each module will include the following minimum test cases:

* Absence of a DUT provides a failing result
* Typical error conditions provide a failing result
* Testing that measurements within range provide a passing result

All test modules will be validated on the test system in its final location using production parts and operators with the same level of education and training that will typically run a test station during manufacturing.

A report will be generated showing at least:

* Date/time
* Operator ID
* Test summary

Test system software will be reviewed by engineers from the Development team and/or the Test team knowledgeable with the software and tests. This review will be documented.

# Software Management

Upon successful verification and validation, product system software/configuration and test system software/configuration shall be managed according to document SWQP 0006.

# Design Verification Test

Due to the complexity of the IPG design, functional manufacturing test systems will be leveraged to build and process the units being used for DVT. The manufacturing test systems will be programmed to allow execution of many or all of the individual tests that make up DVT.

A separate set of test system qualifications similar to IQ, OQ, and PQ protocols will be developed to document and confirm that the test systems function as required in support of first manufacturing builds targeted at DVT activity.

# Revision History

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| --- | --- | --- | --- |
| **Revision Level** | **Revision Description** | **ECN**  **No#** | **Effective**  **Date** |
| 1.1 | Initial Release | 1930 | 09/17/13 |
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